Novel 18/36 GHz (M)MIC GaAs FET Frequency Doublers in CPW-Techniques Under the Consideration of the Effects of Coplanar Discontinuities

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Abstract— **The design and performance of single-device and balanced versions of (M)MIC GaAs FET frequency doublers from 18 GHz to 36 GHz, fabricated in purely coplanar waveguide techniques, are presented. Coplanar discontinuities which are usually neglected are taken into consideration in the analysis and design. Spiral inductors and their associated parasitic capacitance are used for impedance matching and phase shifting purposes. The simulation technique used to characterize the spiral inductors is described in detail. Measurement and simulation results show good agreement. The investigated hybrid doublers have a minimum conversion loss of 7 dB while a maximum conversion gain of 6B is predicted for the monolithic version of the doublers. They are fabricated on ceramic and gallium arsenide substrates and are simple, cost effective, and applicable in low and medium power transmitter/receiver systems.**

I. Introduction

In the last few years the trend of (M)MIC planar circuit design is slowly shifting from microstrips to coplanar waveguides (CPW) for the obvious advantages of the latter over the former [1]–[6]. Small dispersion, simple realization of short circuited ends and the possibility of simple integration of lumped elements or active components are among the advantages that made the coplanar waveguides more attractive for (M)MIC design. Several GaAs FET frequency doublers in K- and KA-band regions using microstrips have been reported [7]–[13]. All of these doublers are relatively large and space occupying. Few (M)MIC doublers operating up to K-band using CPW-techniques have also been reported [2], [3], [15]. To the knowledge of the authors, GaAs FET (M)MIC frequency doublers in KA-band in purely coplanar technology and with the effects of all associated coplanar discontinuities taken into consideration are not yet reported. The design and realization of KA-band (M)MIC doublers in CPW-techniques requires a thorough investigation of the effects of the unavoidable coplanar discontinuities such as bends, T-junctions, crossjunctions, and air bridges. This paper presents the design and realization of such frequency doublers from 18 GHz to 36 GHz in purely CPW technology with the effects of all the discontinuities present in the circuit taken into consideration in the design. Accurate lumped element equivalent circuit models [14], [16] are used to characterize these discontinuities. Moreover, simple spiral inductors and their associated parasitic capacitances are used for impedance matching purposes, thus eliminating the need for the conventionally used metal-insulator-metal (MIM) capacitors. Two different versions of doublers (namely, the single-device and balanced doublers) are investigated and their performances compared. In the balanced doubler version presented here, the conventionally used and space occupying 180-degree hybrid [1, 17] is replaced by small size spiral inductors which are carefully designed to give the desired 180-degree phase shift. The design method will be described in detail. The doublers are fabricated on ceramic and gallium arsenide substrates and there is a quite good agreement between simulation and measurement results.

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II. Design Method

The block diagrams of the doublers investigated here are given in Fig. 1. Since only the second harmonic is of interest for doubler operation all other harmonics must be suppressed. For the single-device doubler of Fig. 1(a), this can be achieved by using either a band-reject filter at the fundamental frequency (a $\lambda/4$ stub as in this case) or a bandpass filter at the second harmonic as part of the output circuit. The lengths l_1 and l_2 indicate the respective location of the filter (stub) and must be optimized for maximum second harmonic output power. In the case of the balanced doubler [Fig. 1(b)] there is no need for utilizing filters since the filtering action for odd harmonics can be achieved by the use of identical transistors connected in push–push operation. For a successful operation of this circuit the 180-degree phase shifter circuit must be accurately designed. Both the single-device and balanced versions are designed and realized in hybrid and monolithic MIC coplanar technology as described in the following sections.

A. Design of the Passive Components

The exact design of the passive components used in the circuit layout is essential to optimize the power output of the

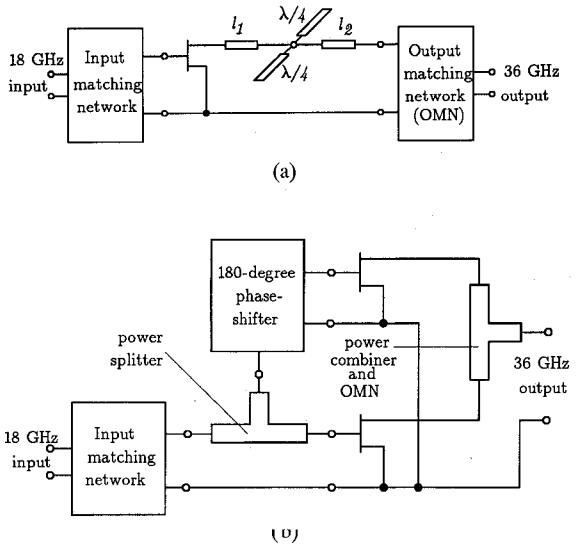

Fig. 1. Block diagrams of the single-device and balanced frequency doublers. (a) Single-device doubler (version A). (b) Balanced (push-push) doubler (version B).

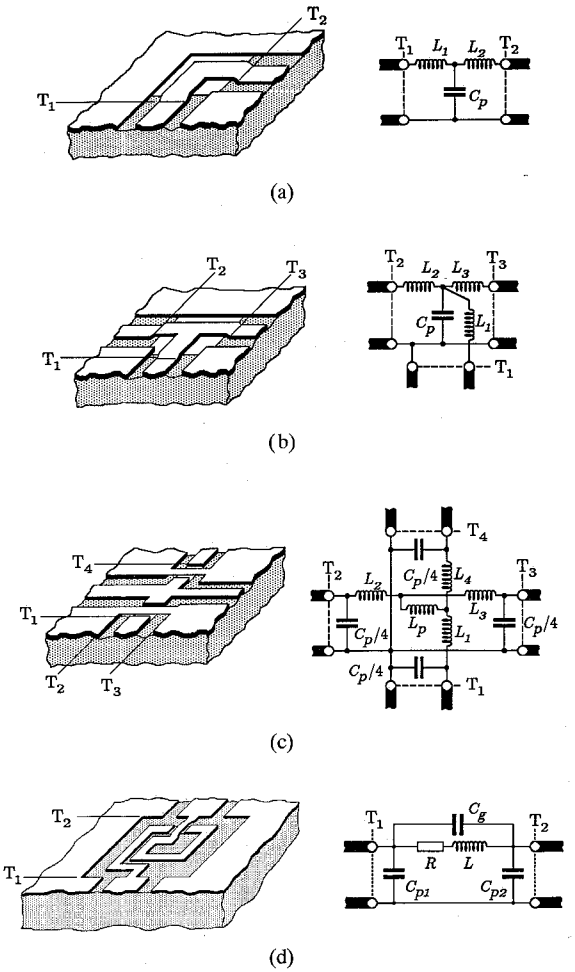

Fig. 2. Coplanar components and their equivalent circuits used in the design. (a) Bend. (b) T-junction. (c) Crossjunction. (d) Spiral Inductor.

doublers at the desired harmonic frequency. The components shown in Fig. 2 are needed for the circuit design. These are:

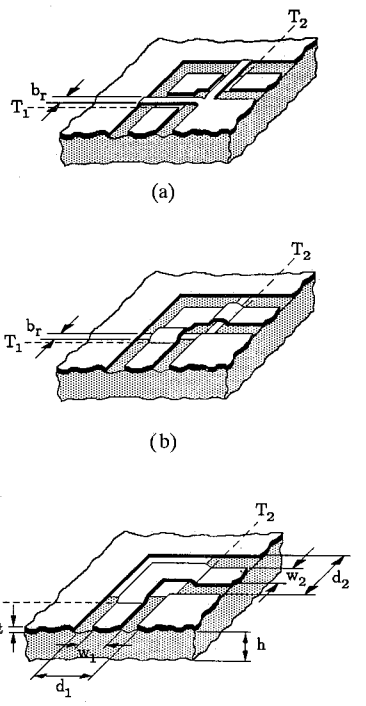

Fig. 3. Three different air-bridge techniques. (a) Air-bridges passing over the inner conductor. (b) Metallic passes under the inner conductor. (c) Connection of the ground planes under the junction.

1) the coplanar airbridge-bend;
2) the coplanar airbridge-T-junction;
3) the coplanar airbridge-cross-junction;
4) the coplanar spiral inductor.

As is well known, the first higher order odd mode is excited at coplanar line discontinuities and this leads to circuit instabilities if it is not sufficiently suppressed. Suppression of this unwanted higher order mode can be accomplished by using airbridge techniques which sufficiently connect the groundplanes of the coplanar structures. Fig. 3 shows three different airbridge techniques which can be used. The technique shown in Fig. 3(c) shows best results considering the odd mode suppression. It can be realized easily using standard airbridge techniques.

In [4] we have shown how the electric fields and the capacitive elements of an equivalent circuit for these three-dimensional (3-D) discontinuities can be calculated using an effective quasi-static finite-difference analysis method. Here, we shall briefly describe how the inductive components of the equivalent circuit can be determined approximately using the same method.

Consider a coplanar discontinuity shown in Fig. 4. If the electric field of this discontinuity is analyzed using quasistatic field relations, the following conditions must be fulfilled:

$$\partial\varphi/\partial x = 0 \quad \rightarrow \quad E_x = 0 \qquad \text{in region I}, \tag{1a}$$

$$\partial\varphi/\partial z = 0 \quad \rightarrow \quad E_z = 0 \qquad \text{in region I}, \tag{1b}$$

$$\partial\varphi/\partial y = 0 \quad \rightarrow \quad E_y = 0 \qquad \text{in region II}, \tag{1c}$$

$$\left.\begin{array}{l}\text{rot } \boldsymbol{E} = \boldsymbol{0} \\ \text{div } \boldsymbol{E} = 0\end{array}\right\} \quad \rightarrow \quad \Delta\varphi = 0 \qquad \text{for } y > 0. \tag{1d}$$

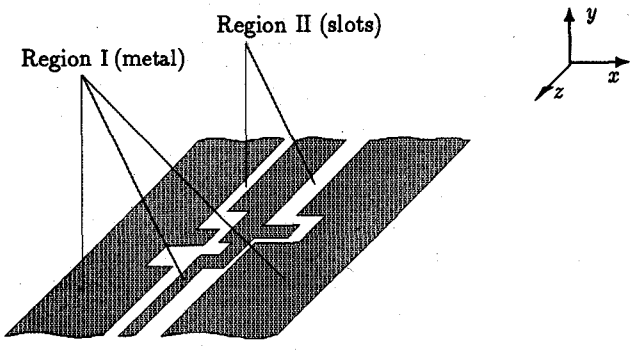

Fig. 4. General schematic diagram of a coplanar discontinuity.

Alternatively the magnetic field of the structure can be analyzed if the following analogy is considered. The total space may be filled with a material of relative permeability $\mu_r = 1$. Because the dielectric properties of the substrate material do not influence the quasistatic field analysis of the magnetic field, the coplanar structure shown in Fig. 4 is symmetric with respect to the metallization plane. Because of this symmetry conditions the magnetic field can be analyzed considering only one half space, e.g., the space above the metallization plane. Under these conditions the magnetic field can be derived from the static potential Ψ, because a current in never included within any arbitrary integration path.

For the magnetic potential Ψ the following relations hold:

$$\partial\Psi/\partial x = 0 \quad \rightarrow \quad H_x = 0 \quad \text{in region II}, \quad (2a)$$

$$\partial\Psi/\partial z = 0 \quad \rightarrow \quad H_z = 0 \quad \text{in region II}, \quad (2b)$$

$$\partial\Psi/\partial y = 0 \quad \rightarrow \quad H_y = 0 \quad \text{in region I}, \quad (2c)$$

$$\left.\begin{array}{l}\text{rot } \boldsymbol{H} = \boldsymbol{0} \\ \text{div } \boldsymbol{H} = 0\end{array}\right\} \quad \rightarrow \quad \Delta\Psi = 0 \quad \text{for } y > 0. \quad (2d)$$

The analogy of (1) and (2) means that the magnetic field of the coplanar structure shown in Fig. 4 can be analyzed using the same finite difference method. This can be done by exchanging the metallized and not metallized areas and then assuming a constant magnetic potential in the slot area of the coplanar structure instead of the constant electric potential in the metallized area used in the case of the electric field. From the so-calculated magnetic potential the magnetic filed strength can be determined. This leads to the current density which can be used to determine the inductive components of the equivalent circuit.

Of course, using this technique, the analysis of the 3-D structures shown in Fig. 2 is only an approximation, because the planar symmetry of the coplanar components is disturbed. But because of the small height of the airbridges ($\approx 3\ \mu$m), the described method can be used with good accuracy. If the method is applied to a spiral inductor, it is exact within the assumption of a quasistatic field analysis.

As an example, Fig. 5 shows the current density distribution in an asymmetrical airbridge-T-junction for three different current excitations at ports 1, 2, and 3, respectively. Fig. 6 shows the comparison between theory and measurement for the scattering parameters of the symmetrical T-junction. It can be recognized that, using the quasistatic equivalent circuit description of the discontinuities including the electric and magnetic effects, a very high accuracy can be reached for frequencies up to 40 GHz and higher.

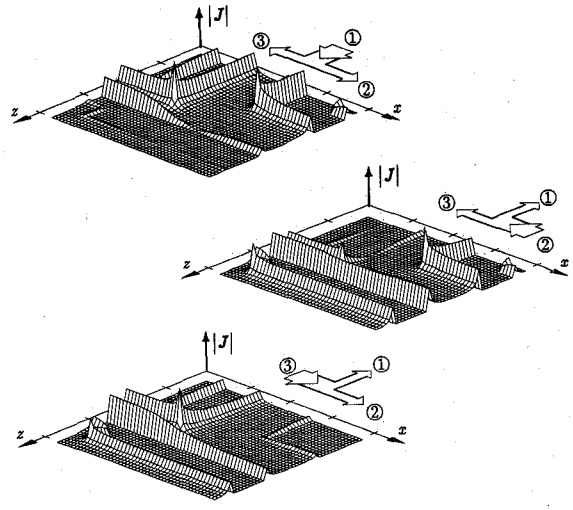

Fig. 5. Three different current excitations of an asymmetrical T-junction.

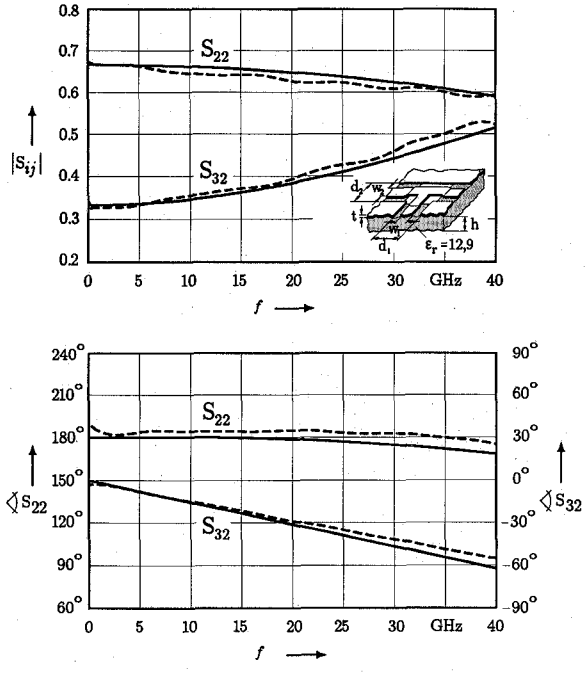

Fig. 6. Measured (dashed lines) and calculated (solid lines) scattering parameters of a symmetrical air-bridge T-junction. ($w_1 = w_2 = w_3 75\ \mu$m, $d_1 = d_2 = d_3 = 175\ \mu$m, $t = 3\ \mu$m, $\varepsilon_r = 12.9$) (Model parameters: $L_1 = 13$ pH, $L_2 = L_3 = 74$ pH, $C_p = 114$ fF).

The analysis of the spiral inductors (including the airbridges from the center of the inductor) needed for the doubler design has been done on the same basis. Fig. 7 shows the spiral inductor and its equivalent circuit. The capacitive elements are calculated from the electric field distribution obtained from the finite difference analysis as described in [4]. The capacitances C_{p1} and C_{p2} are found from an even mode excitation of ports 1 and 2, respectively, ($\varphi_1 = \varphi_2 = 1\ V, \varphi_{\text{ground}} = 0\ V$), the capacitance C_g is calculated using an odd mode excitation ($\varphi_1 = 1\ V, \varphi_2 = -1V, \varphi_{\text{ground}} = 0\ V$).

In Fig. 8(a) the currents and the magnetic potential used for the analysis of the spiral inductor are shown. Fig. 8(b) shows

TABLE I
GEOMETRICAL DIMENSIONS, EQUIVALENT CIRCUIT PARAMETERS AS WELL AS $\lambda/4$ RESONANCE FREQUENCY OF THREE RECTANGULAR COPLANER SPIRAL INDUCTORS.
The resistor $R_f(f)$ in the equivalent circuit is given by:

$$R_f(f) = \begin{cases} R_{dc} + \{R_f(1\text{ GHz}) \cdot \sqrt{f_g/GHz} - R_{dc}\} \cdot (f/f_g) & f \le f_g \\ R_f(1\text{ GHz})\sqrt{f/\text{GHz}} & f > f_g \end{cases},$$

$$f_g/GHz = 39.131 \frac{(\rho/\rho\text{Cu})}{(t/\mu\text{m})} \qquad \rho = \text{resistivity per unit length}$$

$$t = \text{metallization thickness}$$

Parameters	Units	Inductor Number 1	2	3
Number of turns	N	2.5	3.5	4.5
Line-width	w_f/μm	25	25	25
Gap-width	s_f/μm	5	5	5
Inductor-size	$l_x, l_z/\mu$m	185	240	300
Gap to ground	s_m/μm	50	50	50
Gap to ground	s_e/μm	50	50	50
Turn-length	l_{turn}/mm	1.245	2.055	3.155
Model Parameters	L/nH	0.7013	1.455	2.813
	C_{p1}/fF	41.97	60.72	81.34
	C_{p2}/fF	19.03	23.36	29.65
	C_g/fF	21.38	22.16	32.67
	$R_f(1\text{ GHz})/\Omega$	0.334	0.563	0.838
	R_{dc}/Ω	0.434	0.716	1.110
	$f(\lambda/4)$/GHz	30	17	12

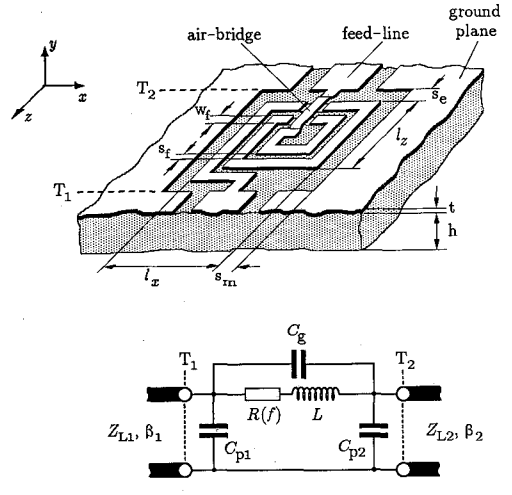

Fig. 7. Coplanar spiral inductor and its equivalent circuit.

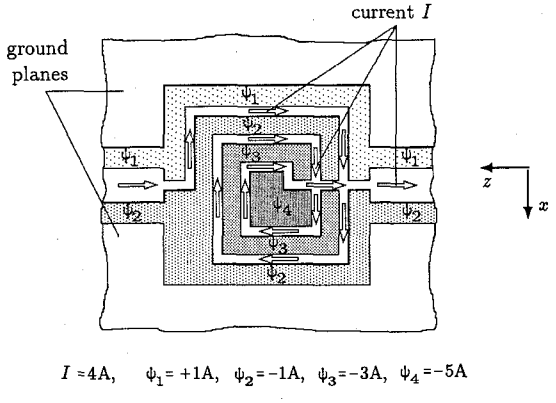

Fig. 8. (a) Current and magnetic potential used for the calculation of the equivalent inductance. (b) Calculated surface current density of the spiral inductor.

the calculated current density within the spiral inductor. Using this current distribution, the resistor of the equivalent circuit can easily be determined. Finally, Fig. 9 shows a comparison between the simulated and measured transmission coefficients S_{21} of three coplanar spiral inductors with the geometrical parameters given in Table I. Again a good agreement between theory and experiment is found, so that a solid basis for the design of the frequency doublers is available.

B. The Hybrid MIC Doublers

NE710 GaAs FET transistors are mounted in coplanar waveguide technique on a ceramic substrate and their S-parameters up to 40 GHz are measured. From the measured DC and S-parameters the necessary model parameters of the transistor are extracted using the Curtice–Ettenberg model for the MESFET [18]. The following transistor equations were used for fitting the measured V/I data to the chosen transistor model:

$$I_{ds} = \left(a_0 + a_1 V_1 + a_2 V_1^2 + a_3 V_1^3\right) \tanh[\gamma V_{\text{out}}(t)] \quad (3)$$

TABLE II
SOME OF THE MODEL PARAMETERS OF THE TRANSISTOR USED IN THE SIMULATION
(CORRESPONDING TO NE710 GaAs FET)

$A\ a_0 = 0.0223\text{A}$	$R_s = 0.64\ \Omega$	$V_{\text{dso}} = 1.0\ V$
$A/V\ a_1 = 0.059\text{A/V}$	$R_d = 1.13\ \Omega$	$R_{\text{dso}} = 1163\ \Omega$
$A/V^2\ a_2 = 0.047\text{A/V}^2$	$R_g = 1.79\ \Omega$	$C_{\text{gdo}} = 0.089\ \text{pF}$
$A/V^3\ a_3 = 0.0118\text{A/V}^3$	$R_{\text{in}} = 0.2\ \Omega$	$C_{\text{gso}} = 0.24\ \text{pF}$
$1/V\ \gamma = 4.0\ 1/\text{V}$	$L_s = 68\ \text{pH}$	$C_{\text{ds}} = 0.07\ pF$
$\beta = 0.04\ 1/\text{V}$	$L_g = 260\ \text{pH}$	$\tau = 2.36\ \text{ps}$
	$L_d = 289\ \text{pH}$	

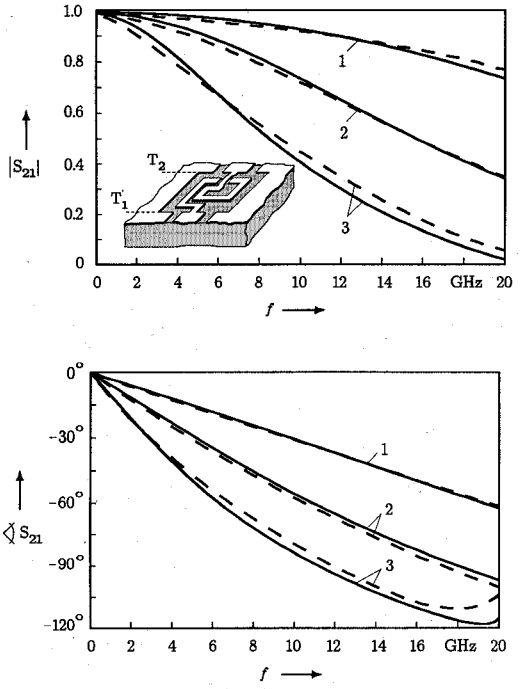

Fig. 9. Measured (- - - - -) and calculated (———) transmission coefficients of three coplanar spiral inductors. (See Table I for dimensions).

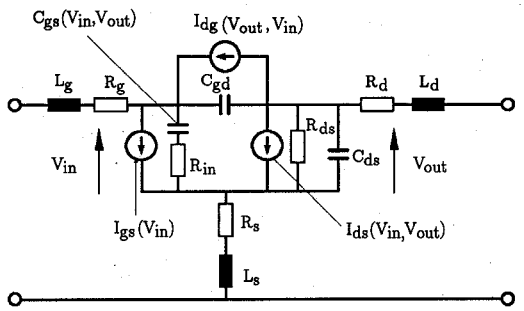

Fig. 10. Used equivalent circuit model of the GaAs FET.

$$V_1 = V_{\text{in}}(t-\tau)\cdot\left[1+\beta(V_{dso}-V_{\text{out}}(t))\right] \qquad (4)$$

where V_1 is the input voltage.

Fig. 10 shows the equivalent circuit of the transistor used and its extracted model parameters are given in Table II.

Two versions of hybrid doublers are investigated. The first one (version A) called the single-device doubler, uses a symmetrical coplanar band-reject stub for harmonic filtering and the spiral inductors described above as matching networks [Fig. 11(a)]. In [5], [6], we explained how the use of

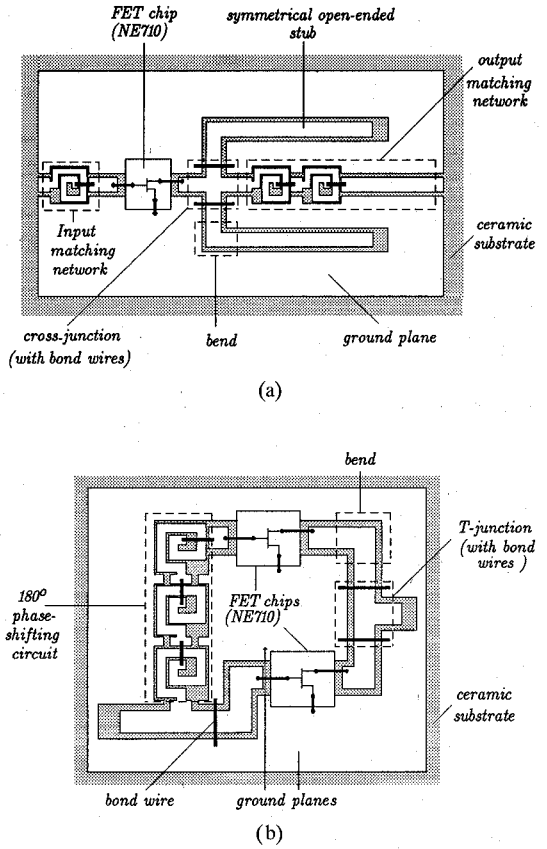

Fig. 11. Layouts of the 18 to 36 GHz hybrid MIC frequency doublers. (a) Single-device doubler. (b) Balanced (push-push) doubler.

symmetrical band-reject stub improves fundamental rejection and also helps to suppress the generation of higher modes without arising the need for using additional bond wires. Moreover, the stub is bended in order to minimize its size. The parasitic capacitances of the spiral inductors are too large to be neglected at the operating frequency and infact are exploited in the design to serve as part of the matching elements. For the coplanar band-reject stub bond-wires are necessary to keep the coplanar ground planes on both sides of the crossjunction at the same potential [Fig. 11(a)]. The problem with the realization of such a circuit is that the resonance frequency is influenced by the length and location of the bond wires used [5], [6] and hence there is a difficulty reproducing the circuit accurately. The second disadvantage is that the stub occupies a relatively large space.

To overcome the above mentioned problems a second type of doubler (version B) is proposed; namely, the push–push

TABLE III
USED COPLANAR LINE DISCONTINUITIES AND PARAMETERS OF THEIR EQUIVALENT CIRCUITS

Microwave components	Geometrical dimensions	Equivalent circuit values
Bend	line-widths: $w_1 = w_2 = 75\ \mu$m slot-widths: $s_1 = s_2 = 50\ \mu$m bridge height = 3 μm	$L_1 = L_2 = 0.01443\ nH$ $C = 0.0265$ pF
T-junction	line-widths: $w_1 = w_2 = w_3 = 75\ \mu$m slot-widths: $s_1 = s_2 = s_3 = 50\ \mu$m bridge height = 3 μm	$L_1 = 0.0069$ nH $L_2 = 0.052$ nH $L_3 = 0.051$ nH $C = 0.111\ pF$
Crossjunction	line-widths: $w_1 = w_2 = w_3 = w_4 = 75\ \mu$m slot-widths: $s_1 = s_2 = s_3 = s_4 = 50\ \mu$m bridge height = 3 μm	$L_1 = 0.041$ nH $L_2 = 0.033$ nH $L_3 = 0.033$ nH $L_4 = 0.041$ nH $L_p = -0.013$ nH $C_p/4 = 0.013$ pF

doubler [Fig. 11(b)]. This doubler is more compact and has less conversion loss. The push–push (balanced) doubler proposed here does not utilize the conventionally used and space occupying 180-degree coupler [1], [17]. Instead, simple spiral inductors and their parasitic capacitances are used to obtain the desired 180-degree phase shift between the gates of the two transistors. The necessary number of spiral inductors and the corresponding windings required for the phase-shifting must be properly optimized using the above described design methods. In this way the fundamental frequency at the output will be suppressed and the second harmonic is enhanced. Optimum second harmonic generation is obtained when the transistors are biased near pinchoff. Operating near pinchoff has also the advantage of improving the DC to RF efficiency.

C. The Monolithic MIC Doubler

The advantages of MMIC technology are well known [1], [3], [7], [15], [19]. Design reproducibility and compactness of the circuit are among its advantages. To this end, the designs of the doublers mentioned in Section II-B are repeated in an MMIC coplanar technology on a GaAs substrate. The layouts are shown in Figure 12(a) and 12(b). A 0.3 micron gate length and 200 micron gate width GaAs FET transistor is used for the design. The nonlinear model for the transistor is constructed using the Curtice–Ettenberg model [18]. From the measured DC and S-parameters the model parameters are determined. The effects of the associated crossjunctions, T-junctions, bends, and air bridges are taken into account in the simulation of the circuits. This is done by replacing them with the accurate lumped element equivalent circuit models shown in Fig. 2 to characterize the coplanar discontinuities [4], [16]. Table III summarizes the component values used in the simulation corresponding to some of the microwave components listed in Fig. 2. In the case of the single-device doubler output power is influenced by the length l_1 of the coplanar line between the band-reject filter (stub) and the drain of the transistor. The optimum value of l_1 is found to be 415 μm. Fig. 13(b) shows the dependence of the output power on the location (l_1) of the stub with respect to the drain

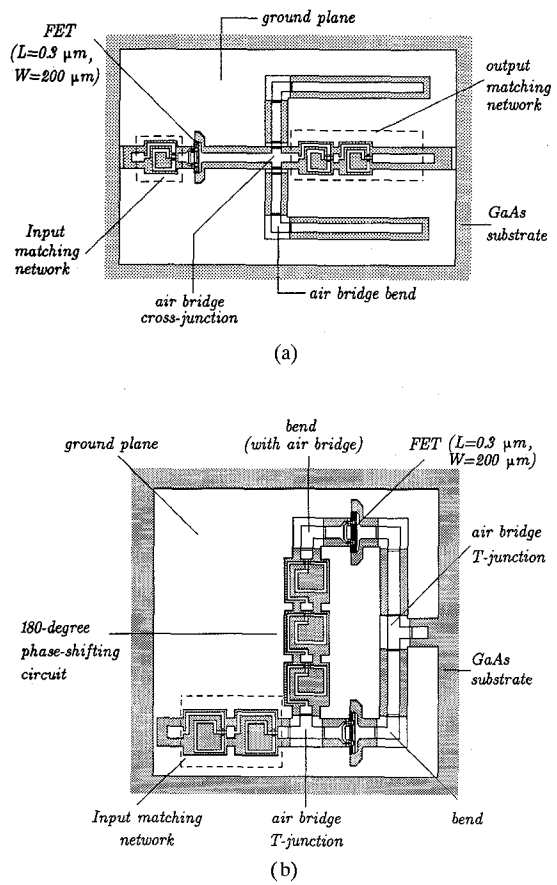

Fig. 12. Layouts of the 18 to 36 GHz monolithic MIC frequency doublers. (a) Single-device doubler. (b) Balanced (push–push) doubler.

of the transistor. One version of the MMIC balanced doubler including the matching networks and the 180-degree phase shifting circuit occupies a space of 1.5 × 1.5 mm^2. Its layout is shown in Fig. 12(b).

The monolithic band-reject filter at 18 GHz is at first fabricated separately and is found to resonate at the desired frequency. The effects of the crossjunction and bends associated with this filter are taken into account in the design. It is then incorporated into the output matching network and the

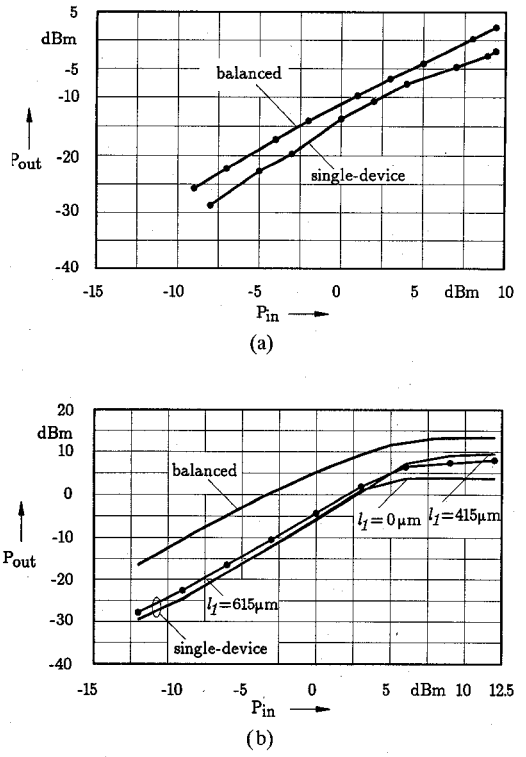

Fig. 13. Output power comparison of the balanced and single-device (M)MIC doublers. (a) Hybrid (measurement). (b) Monolithic (simulation), where l_1 is the length of the coplanar line between the drain and the band-reject filter

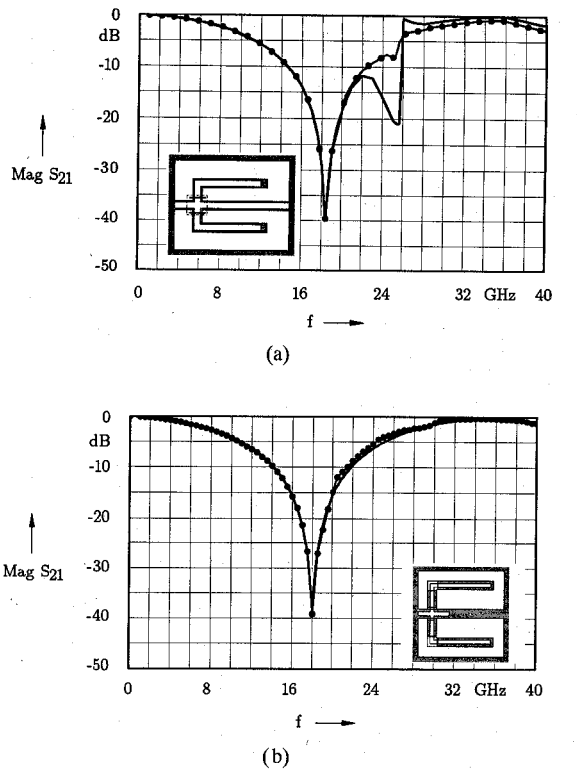

Fig. 14. Measured (· · · · · ·) and calculated (———) rejection levels of the band-reject filters. (a) Hybrid. (b) Monolithic.

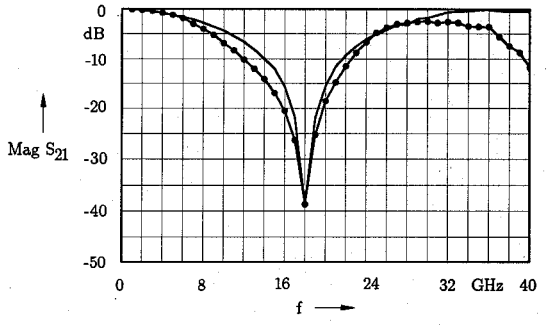

Fig. 15. Measured transmission coefficients of the monolithic band-reject filter with (· · · · · ·) and without (———) the output matching networks.

combined performance is investigated. Several such circuits are fabricated on a gallium arsenide substrate and measurement results proved the reproducibility of the design (Figs. 14(b) and 15)

III. Results

Fig. 16(a) shows the simulated and measured output power (36 GHz) of the single-device doubler (version A) for different input power levels. It shows a minimum conversion loss (CL) of 10 dB. A 3 dB improvement in the conversion loss (i.e., CL = 7 dB) is achieved if the balanced doubler (version B) of Fig. 11(b) is used. Its measured and simulated results are shown in Fig. 16(b). The second harmonic and the fundamental power levels at the output of the balanced doubler for different values of input power are compared in Fig. 17. It has been observed that the fundamental power level lies 19 dB below that of the second harmonic power level for the case of the balanced hybrid doubler and 15 dB for the case of the single-device hybrid doubler. The single-device and balanced doublers are compared in Fig. 13. Figure 13(b) shows the dependence of the output power on the length l_1 of the coplanar line between the band-reject filter and the drain of the transistor. The conversion loss and second harmonic output powers are optimized with respect to the bias voltage. Figures 18 and 19 show, respectively, the dependence of the conversion loss (or gain) and the output power on the bias point of the transistor. From the simulation results of Fig. 19(b) we observe that the balanced monolithic MIC doubler has a maximum predicted conversion gain of 6 dB (for measurement results see [20]). The desired 180-degree phase shifting is successfully achieved by the properly designed spiral inductors. This is demonstrated in Fig. 20. Several such 180-degree phase shifters have been fabricated on ceramic and gallium arsenide substrates and proved to be reproducible. Fig. 14 shows the measured and calculated transmission coefficients (rejection levels) of both the hybrid and monolithic band-reject filters. The measured performance of the monolithic band reject filter with and without the matching network are compared in Fig. 15.

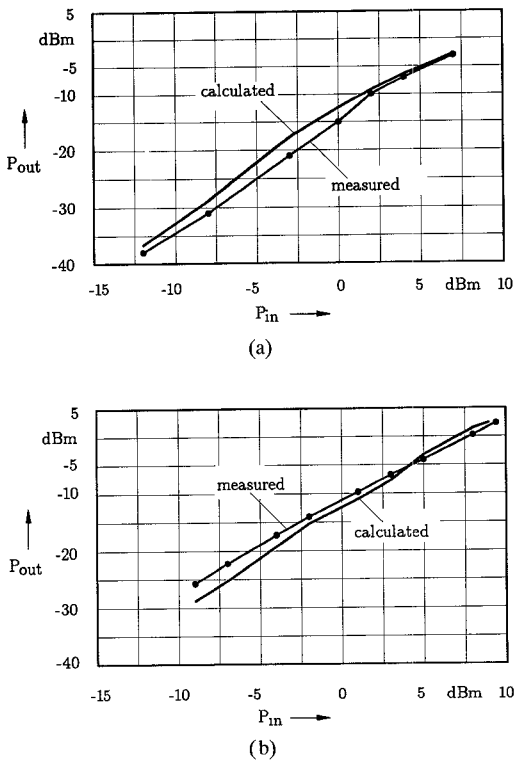

Fig. 16. Measured and calculated results of the hybrid MIC doublers. (a) Single-device (Version A). (b) Balanced (Version B).

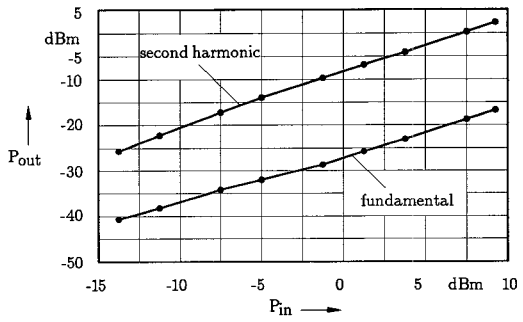

Fig. 17. Comparison of the measured fundamental and second harmonic power levels at the output of the hybrid balanced doubler.

IV. Conclusions

Single-device and balanced frequency doublers in KA-band are designed and fabricated on ceramic and gallium arsenide substrates in purely coplanar (M)MIC technology. The effects of the coplanar discontinuities are taken into consideration in the design. The calculated and measured results are in good agreement. The doublers have a minimum conversion loss of 7 dB and are small in size, cost-effective, and are applicable in small and medium power transmitter/receiver systems.

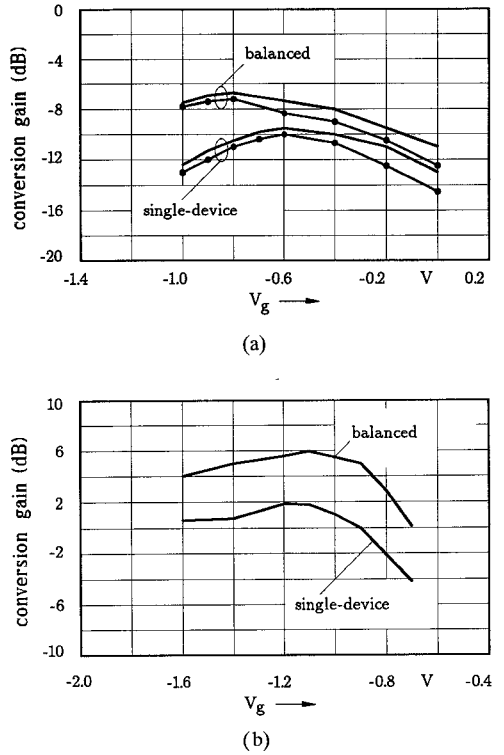

Fig. 18 (a) Measured (· · · · · ·) and simulated (———) conversion losses of the hybrid doublers as a function of bias voltage. (b) Simulated conversion gain of the monolithic doublers as a function of bias voltage. (All the results correspond to an input power of 6 dBm)

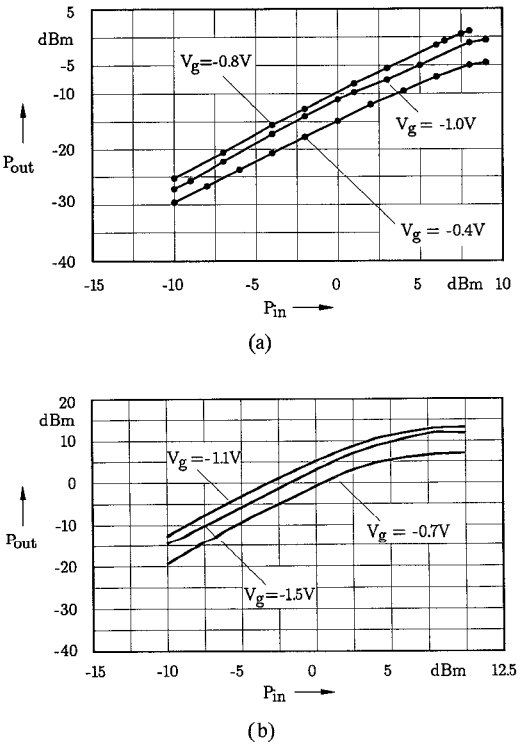

Fig. 19. Dependence of the second harmonic output power on the input power with the bias voltage as a parameter. (a) Hybrid balanced doubler (measurement). (b) Monolithic balanced doubler (simulation).

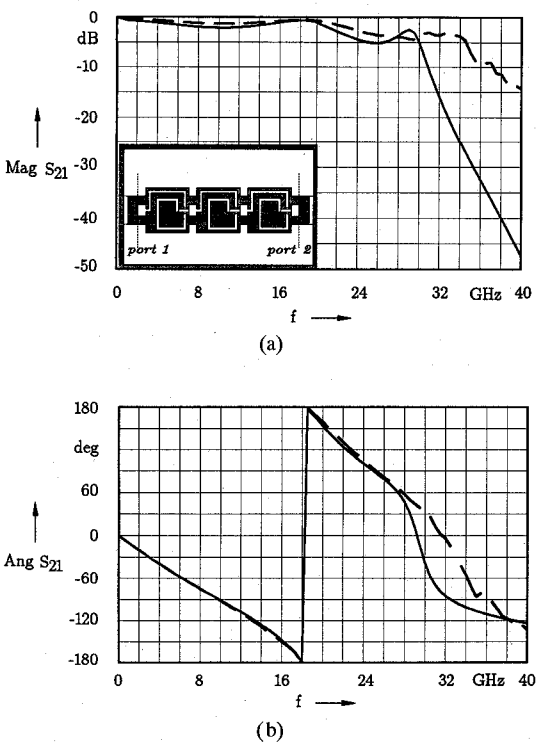

Fig. 20 Measured (- - - - -) and calculated (———) transmission coefficients of the 180-degree phase-shifting circuit on a GaAs substrate. (a) Magnitude. (b) Phase angle.

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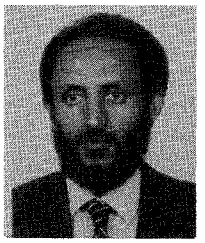

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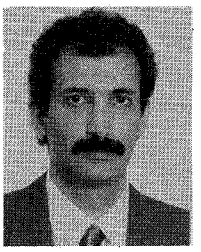

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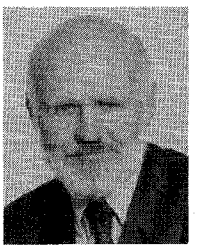

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